Role of an Individual Grain Boundary in Thermal Transport across Single Crystalline CVD Graphene

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THESIS

Submitted as partial fulfillment of the requirements for the degree of Master of Science in Mechanical Engineering to the Graduate College of the University of Illinois at Chicago, 2014

Chicago, Illinois

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To my parents,

To my loving wife, Shokoufeh

To my sisters Neda, and Nasim

And to my friends.
ACKNOWLEDGMENTS

This thesis paper could not be written without the help and support of Dr. Amin Salehi-Khojin, who served as my supervisor, gave me support and assistance, and provided me with motivation and encouragement throughout the entire period of my research work at the Nanomaterials and Energy Systems Laboratory. My deepest gratitude goes also to my family and friends for their moral support. I also wish to thank Mohammad, Bijandra, Poya, and Amir who helped me to complete this thesis.
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SUMMARY

Graphene is a one atom thick sheet of carbon, joined together in a honeycomb structure. It is being considered as a way to overcome some of technological limitations of silicon in integrated circuit industry owing to its extraordinary electrical, mechanical and thermal properties.

The most promising method to fabricate graphene in a large scale is through Chemical Vapor Deposition (CVD). However, CVD graphene is only available in polycrystalline form. In polycrystalline graphene, the single crystalline regions are joined together making grain boundaries which govern the physical properties of CVD graphene. It has been shown that the electrical properties of graphene are highly affected by the temperature. Therefore, it is important to understand physical phenomenon behind the thermal transport across polycrystalline graphene. In this respect, the role of grain boundaries on the thermal transport of graphene must be extensively explored.

In this work, large area single crystalline graphene flakes with detectable grain boundaries are grown on copper substrate using atmospheric pressure CVD. An electrical thermometry platform is then design in order to simultaneously measure the thermal conductivity of a single crystalline graphene flake as well as an individual grain boundary formed between two graphene flakes. It was shown that an individual grain boundary acts as an effective 1.24 $\mu$m extension in length of the single crystalline graphene at room temperature which results in an average of 26% overall reduction of thermal conductivity. Also, the thermal
conductivity of an isolated grain boundary is found to be around 3 orders of magnitude smaller than that of the graphene on Silicon Nitride substrate.
CHAPTER 1

INTRODUCTION

1.1 The Rise of Graphene

Graphene is a two dimensional sheet of carbon atoms joined together in a honeycomb structure that demonstrates extraordinary electrical, mechanical, and thermal properties [1-3]. The properties of such a 2D material were first theoretically predicted in 1947 as a basic study of the electronic structure of 3D graphite. In 2004, Andre Geim and Konstantin Novoselov [1] were able to successfully fabricate graphene using a simply mechanical exfoliation method that won them the Nobel Prize of 2010. Exfoliation of graphene indeed revolutionized the 21 century research studies. Thousands of articles have been published ever since, all reporting extraordinary results, unseen in any other material known to man. The carrier mobility of 5000 $cm^2V^{-1}S^{-1}$ was reported for graphene that is a record among semiconducting materials [4]. Also 1 $TPa$ Young modulus [2] and more than 3000 $W/mK$ thermal conductivity [3] is observed for a monolayer sheet of graphene.

Apart from the basic properties, the two dimensional nature of graphene has resulted in direct observation of many interesting quantum mechanical properties. For instance, the electronic band structure of graphene has an overlapping conduction and valence band at a singular point known as the Dirac point [5]. The linear energy dispersion relation around Dirac point of graphene electronic band structure has resulted
in the first direct observation of two dimensional massless Dirac fermions travelling very close to the speed of light ($10^6 \text{ m/s}$ Fermi velocity) [5-7]. The transport behavior such massless subatomic particles can only be explained through quantum relativistic equation that accommodates the massless particles traveling at very high speeds.

Graphene has also found direct application in the area of toxic gas molecule detection [8-10]. The large, planar surface area and extremely high electrical mobility of graphene has made it one of the leading materials in field. The electrical resistance of graphene has shown significant sensitivity toward gas molecules, resulting in production of graphene based micro chemical sensors. Detection of an individual gas molecule has been reported using single crystalline graphene upon exposure of 1 ppm (part per million) of NO$_2$ gas molecules [11].

These extraordinary mechanical, thermal, electrical, and quantum mechanical properties in graphene have made it one of the most attractive materials mankind ever came to know.

1.2 Future of microprocessors

According to Moore’s law, the transistor count per chip doubles every two years [12]. Shrinkage in size and increase in transistor count per chip, however, is pushing the silicon based industry toward its physical limitations. Graphene is a potentially attractive electronic materials, in that it has record carrier mobility and critical dimensions that are in the atomic scale [4][13]. It is being widely explored as a way of overcoming the
technological and fundamental limitations of silicon-based electronics at the atomic scale. However, the physical properties of graphene depend on temperature [14], and thus its performance is directly affected by heat dissipation during electrical operation. Uneven thermal maps and “hot spots” can cause physical stress on the graphene surface and consequently will breakdown the system [15][16]. These problems are likely to grow far worse as the demand is growing for decreased feature size, increased packaging densities and increased functionality of the electronic devices. These issues make thermal management and cooling of carbon-based electronic devices crucial for the enhanced performance, reliability and durability of nanoelectronic devices. In this respect, efforts are required to explore the limitation of graphene toward the path of industrialization.

1.3 Toward the Replacement of Graphene with Silicon in Integrated Circuits

In order to fabricate graphene for industrial application, few problems need to be overcome. First of all, the band structure of graphene has an overlapping conduction and valence bands in a singular point, making graphene a semimetal rather than semiconductor [17]. Lack of a band gap in the electronic structure of graphene results in very high leakage current consequently an inefficient device. A band gap can, however, be implemented into the graphene structure through dimensional confinement that is fabricating ribbons of graphene with less than 100 nm in width [18-20]. Although this method results in lower mean free path of the carriers [21], the properties are still competitive to those of silicon.
The second problem toward industrialization of this material is the mass production of monolayer films of graphene. In mechanical exfoliation technique, the weak bonds between the bulk carbon layers of single crystalline graphite are peeled off using a typical scotch tape [1]. The graphene is then transferred to a receiving substrate by putting the scotch tape on the surface and removing it very slowly. Afterwards the graphene flakes need to be located using an optical microscope. Typical flake size of Mechanical exfoliated graphene is around 1-3 \( \mu m \) (square root of the flake area). Despite the great quality of the graphene obtained from mechanical exfoliation, the production yield of this method is extremely low since the single layer graphene flakes are exfoliated in random locations. Finding a monolayer flake typically takes from 40 min to an hour in the eye of an expert. Besides, industrialization of graphene requires a large area production technique which the scotch tape method is incapable of providing. For these reason, mass production of graphene is not feasible through mechanical exfoliation.

Other efforts are taken to directly grow monolayer graphene using Chemical Vapor Deposition (CVD) technique [22]. In CVD method, large film of graphene is grown on a copper foil which can be transferred to any substrate through a standard transfer process (discussed in chapter 3). Although CVD grown graphene at first seemed to have all it takes for graphene to go to the next level, studies revealed that its electronic properties are greatly altered during the CVD growth process [23]. The reason for this observation was that the CVD graphene suffers from polycrystallinity. Properties of polycrystalline graphene are governed by the level of defects, amount of wrinkles, and
most importantly grain boundaries (GB) joining the single crystalline areas. Although the
effect of GBs on the electronic transport of graphene is widely explored [24-26], much
less is known about their role on the thermal transport across the lattice.

1.4 Importance of Graphene thermal transport from Energy Saving Perspective

Energy consumption in the world is having an upward trend. As shown in figure
1, the statistical analysis project over 40% increase in the overall energy consumption of
the world by 2040 [27]. United States is one of the major energy consumers of energy,
currently responsible for more than 18% of the overall energy consumed worldwide [27].
This makes US a major producer of greenhouse gases in the world and one of the greatest
contributors to the global warming. Therefore, US have a critical need to improve the
efficiency of power generation and consumption.

More than 5% of the energy in the US is consumed by electronic devices such as
personal computers, laptop and smart phones [28]. This trend is likely to increase since
by advancements in technology as new wearable electronic devices are being introduced
to the world every day [29]. Most of the power consumption in such electronic devices is
caused by their microprocessors. The consumption of microprocessors is often affected
by temperature as the leakage current is increased with temperature. Therefore,
temperature rise in the conducting channel of the microprocessors (due to joule self-
heating) greatly alters their energy efficiency [16][30]. For this reason, as graphene is
considered the next generation of microprocessors, it is critically important to understand
the physical phenomena behind its thermal transport and power dissipation regimes. In particular, the role of an individual graphene GBs on the overall heat dissipation of the system needs to be extensively studied as CVD graphene contains many GBs.

1.5 Research Objective

In this study, a method is proposed in order to overcome the technological difficulties of exploring the grain boundaries of a CVD grown graphene film. Atmospheric Pressure CVD is employed in order to grow graphene flakes with detectable GBs. Next, an electrical thermometry platform is designed, and fabricated on a 75 nm thick Silicon Nitride membrane using advanced micro- and nano-fabrication techniques. The thermometry platform is employed in order to measure the thermal conductivity across two single crystalline graphene flakes joined by an individual GB.
Figure 1. World’s current and projected energy consumption per year. [27]
CHAPTER 2

CHEMICAL VAPOR DEPOSITION OF LARGE AREA SINGLE CRYSTALLINE GRAPHENE FLAKES WITH DETECTABLE GRAIN BOUNDARIES

2.1 Introduction

As mentioned in chapter 1, the most promising method for large scale fabrication of graphene is Chemical Vapor Deposition (CVD). However the graphene grown using this method contains many single crystalline domains joined by Grain Boundaries (GB) that govern the properties of the graphene film. Although many efforts are taken into fabrication of graphene with large flake sizes [31-36], much less is known about the properties of their GBs. The performed studies were mainly focused on the electrical and structural properties of GBs [24-26][37]. Therefore, the thermal properties of graphene GBs are yet to be explored. The main technological challenge on studying the graphene GBs is to have a proper method for locating them. For this reason, a method is provided in this chapter to grow graphene flakes on copper foil with large grain sizes, making it possible to detect the GBs using optical or electron microscopy methods.

2.2 Existing methods for detection of graphene grain boundaries

Doung et al. [38] suggested exposure of GBs to oxygen (O) and (OH) radicals is a possible way to probe the GBs of a graphene film on copper foil since the GBs are the first regions to burn due to their defective nature. However, oxidation of GBs is a
destructive method preventing any further analysis after the GBs are located. Other studies suggested Annular Dark-Field Scanning Transmission Electron Microscopy (ADF-STEM) and Dark Field Transmission Electron Microscopy (DF-TEM) in order to image the mono-crystalline regions of a CVD grown graphene film and to obtain atomically resolved images from the GBs. The graphene domains in this technique are separately imaged using an objective aperture filter in the back focal plane that allowed the collection of electrons diffracted in a particular angle. This technique provides information about only a single in-plane crystallographic orientation of the graphene interface (i.e. single grains). Therefore, by repeating this process for various filters and overlaying the images of each run, the shapes of polycrystalline graphene grains were obtained indicating the position of the GBs [39][40]. Despite the accuracy and great resolution of this method, problems such as carbon contamination and difficult sample preparation remain unsolved. Also a handful of studies employed ultra-high vacuum Scanning Tunneling Microscopy (STM) to locate and characterize graphene GBs both on copper and silicon oxide (SiO$_2$) substrates [41][42]. However, due to the very small field of view in STM, locating GBs relative to a predefined alignment mark is again very difficult. Besides, other problems such as obtaining an atomically clean surface or electrical insulation of the substrate (on SiO$_2$) together with high cost of this method, makes it a challenging and time consuming experiment.
2.3 Atmospheric versus Low pressure CVD graphene

Chemical Vapor Deposition (CVD) is a thin film growth technique in which certain kind of gases are purged into a chamber at very high temperatures. A desired film is then formed on a catalyst surface during a series of chemical reactions after decomposition of gas species. In many cases, a mixture of different gases at various temperatures is purged in order to achieve a specific film. Mass flow controllers and a mixing chamber are usually employed to precisely control the flow of gases. It should be noted that since the films are grown during a chemical reaction, all the environmental condition such as temperature, pressure, furnace contamination and purity of the gases can effectively change the quality of the films. For this reason, grow of monolayer graphene using CVD is a challenging process and varies from furnace to furnace and the growth parameters (temperature and flow of gases) must be precisely controlled.

Graphene is typically grown on copper foil (catalyst) using two types of chemical vapor deposition processes; namely Low Pressure (LPCVD) and Atmospheric Pressure (APCVD). In LPCVD a mechanical pump is usually used to evacuate the chamber of any contamination and gases down to \( \sim 1 \text{ mTorr} \) and continues on working during the entire process, while in APCVD the reaction happens at atmospheric pressure. Monolayer graphene films obtained from LPCVD often consist of relatively small (<1um) single crystalline domains that usually take random shapes or complex shapes [32][40]. By the aid of APCVD, however, it is possible to achieve single crystalline graphene grains of sub-centimeter size [43][44]. The flakes obtained from a well-controlled APCVD process
are hexagonal in shape with zigzag edges [37]. The graphene used in this study is grown using APCVD since the task of detecting GBs favors large area flakes with a definite shape.

Our approach toward obtaining a CVD grown film with detectable GBs is by controlling the number of nucleation sites and the size of the single crystalline regions during the APCVD graphene growth process. Nucleation site are points where a graphene flake starts growing from. If there are not too many nucleation sites, hexagonally shaped graphene flakes would only partially cover the surface area. Therefore, it is possible to detect the GBs of such a graphene film as they are simply located at the merging region of two neighboring flakes.

2.3 Growth Process, Characterization and Detection of Graphene grain boundaries

Figure 2a and 2b show the image and schematic illustration of our three zone MTI model OTF-1200X CVD furnace. The oil trap after the exhaust of the furnace is manual embedded in order to prevent any oxygen from diffusing back into the system during the atmospheric growth. Before having the oil trap, any attempt on growing graphene in atmospheric conditions failed since existence or diffusion of any oxygen specie to the furnace results burns the entire grown graphene film. For consistency, the regulator pressures of each gas cylinder are calibrated with pressure gauge of the furnace at 1 atmosphere.
Figure 02. (a) Chemical Vapor Deposition system. (b) Schematic illustration of our CVD system components.

There are three species used in graphene growth; Methane (CH₄), Hydrogen (H₂) and Argon (Ar). The copper foil used in our growth process is purchased from Alfa Aesar (product no. 46365). Special treatments are performed on the copper foils prior to loading them into the furnace in order to control the number of nucleation sites. First, the
foils are cut to proper sizes (fitting the furnace), cleaned with acetone, rinsed with deionized water (DI water). Next they are placed inside a 10% diluted Hydrochloric acid (HCL) solution for 10 min. Acid treatment helps on removing any local oxidation of the copper foil. The treated copper foils are then rinsed with DI water, cleaned with acetone followed by isopropanol (IPA) and DI water again. After rapidly drying them under N₂ flow, the foils are loaded into the 3.14” quartz CVD furnace tube and the system is immediately evacuated to ~1 mTorr to remove all the oxygen content from the system. There are mainly three species used in graphene growth; Methane (CH₄), Hydrogen (H₂) and Argon (Ar). After the evacuation of the furnace, the pump is turned off and the system is purged with forming gas (5% hydrogen diluted in argon) to reach atmospheric pressure. The exhaust valve is then opened allowing the flowing the gases out of the tube and through the oil trap. The sample to then heated up to 1050 °C under the protection of forming gas and annealed for 60-90 minutes in order to anneal the copper foil surface. The growth starts taking place by introducing 20 ppm CH₄ for a short period of time to obtain desired grain size and surface coverage. The furnace is then rapidly cooled down (furnace lid is opened) to room temperature in protection of forming gas. Unfortunately, the growth time for achieving a perfect partial coverage and grain size tend to change from time to time. For this reason few trials may be required in order to obtain the desired graphene film with detectable GBs. The typical grow times are between 60 min to 90 min.
The hexagonally shaped feature of the grown flakes enables us to identify two merged grains using scanning electron microscope (SEM) or by simple optical microscope with an optimized CCD camera. Figure 3a show an optical image a typical partially covered, hexagonally shaped graphene film on SiO$_2$ substrate.

The next question to address is whether the hexagonally shaped graphene flakes are in fact single crystalline. For this reason, we perform transmission electron microscopy (TEM). Figure 3b shows the selected area electron diffraction (SAED) patterns of the flakes obtained for both grain and GB regions. Identical and sharp hexagonal diffraction patterns recorded for the grains in different regions confirm their single crystalline nature. However, a twofold diffraction patterns was observed when the aperture was located exactly at the merging region disclosing a crystallographic mismatch between the grains, evidencing the existence of GBs. Also, in collaboration with Professor Yong P. Chen group in Purdue University, a high spatial resolution Raman map of our graphene flakes are obtained. D-band (I$_D$) Raman map of two merged grains is shown in figure 3c. This map clearly shows the existence of a GB in the form of defects at the merging region of the flakes. The defective spots around the center of the flakes may be attributed to the nucleation sites or the defects introduced during the transfer process. Also, high peak ratio (>2.5) of the 2D and G bands (I$_{2D}$/I$_G$) in figure 3d shows that the flakes are monolayer and have good quality [45]. The Raman maps were achieved using a Horiba Jobin Yvon XploRa confocal Raman microscope equipped with a motorized sample stage from Marzhauser Wetzlar. The laser excitation wavelength of
532 nm is used to obtain the maps of graphene flakes on SiO$_2$ substrate. For the D, G and 2D-peak spatial maps, the wavenumbers of $\sim$1350 cm$^{-1}$ (D), $\sim$1580 cm$^{-1}$ (G) and $\sim$2690 cm$^{-1}$ (2D) were used, respectively. The spectral resolution of the laser is 2.5 cm$^{-1}$, and pixel size of the map is 500 nm. The maps are in good consistency with the previously reported Raman maps of hexagonally shaped graphene flakes [37]. Details of the transfer process of graphene flakes to an arbitrary substrate are discussed in chapter 3.
Figure 3. (a) Optical image of hexagonally shaped graphene flakes randomly merged, making a grain boundary. The scale bar is 20 μm. (b) Identical SAED pattern for the graphene flakes ($G_L$ and $G_R$) obtained from several location of their grain region and twofold SAED pattern obtained from their GB. (c) D-peak Raman map of two typical flakes. (d) 2D- to G-peak intensity ratio Raman map of the flakes. The scale bars of (c) and (d) are 5 μm.
2.4 Role of H\textsubscript{2} in CVD graphene growth process

So far, a method is describes in order to grow large area, hexagonally shaped, single crystalline graphene using APCVD. As mentioned earlier, three kinds of gases are used during the graphene growth. Methane is used as a source of Carbon specie, and Argon is only a carrier gas. However, H\textsubscript{2} plays a much more critical point in final size and shape of the grains. The role of H\textsubscript{2} in graphene growth is extensively studied by ref [46] and [47]. In this section a brief summary of these works together with our own observations on the role of H\textsubscript{2} is discussed. Understanding the role of H\textsubscript{2} is crucially important if perfect 6-fold hexagonal graphene grains are targeted.

Without H\textsubscript{2}, the graphene growth relies on chemisorption of CH\textsubscript{4} specie with the copper foil through the following chemical reaction:

\[ Cu + CH_4 \rightarrow (CH_3)_s + H_s \]  

(2.1) [47]

Formation of a surface-bound active Carbon from (CH\textsubscript{3})\textsubscript{s} is a thermodynamically unfavorable process resulting in very small or no growth. In presence of H\textsubscript{2}, however, formation of (CH\textsubscript{3})\textsubscript{s} radicals is facilitated as the physisorbed methane species on the copper surface ((CH\textsubscript{4})\textsubscript{s}) can be reduced to surface-bound active carbon species through following reactions in a thermodynamically favorable manner:

\[ Cu + H_2 \leftrightarrow 2H_s \]  

(2.2) [47]

\[ (CH_4)_s + H_s \leftrightarrow (CH_3)_s + H_2 \]  

(2.3) [47]

Despite the role of H\textsubscript{2} as a surface activation agent, it is also observed that the content of H\textsubscript{2} directly controls the shape of the grains. At low H\textsubscript{2} partial pressures, irregularly
shaped graphene flakes are obtained, while very high H$_2$ pressures result in very small or no graphene flakes. However, by precisely controlling the amount of H$_2$, perfect hexagonal flakes with grain sizes of up to 50 µm may be obtained. This behavior of H$_2$ is mainly due to its second role in the growth process that is etching the weakly bonded Carbon atoms from the graphene film through the following reaction:

$$H_s + \text{graphene} \leftrightarrow (\text{graphene} - C) + (CH_x)_s \quad (2.4)$$

As shown in reaction (2.4), H$_2$ subsequently reacts with the graphene, and etch the weakly bonded carbon atoms. Figure 4 shows the optical image of the graphene flakes obtained in a high H$_2$ flow. As the image clearly shows, the defective parts (i.e., GBs) are etched away by H$_2$ due to their weaker bonding. Thus, growing continues graphene flakes with detectable GBs is only possible by precisely controlling the contents of H$_2$.

![Graphene flakes obtained in excessive hydrogen flow. Excess of hydrogen during the growth etches the defective part of the flakes, leading to discontinues film. The scale bar is 10 µm](image)

Figure 4. Graphene flakes obtained in excessive hydrogen flow. Excess of hydrogen during the growth etches the defective part of the flakes, leading to discontinues film. The scale bar is 10 µm
2.5 Conclusion

A cost effective and non-destructive method for detection of graphene GBs grown in APCVD process is provided. The employed strategy is to grow a partially covered, large area hexagonal graphene flakes that randomly merge into each other forming a GB. Role of hydrogen in the APCVD growth of graphene on copper is discussed. It is shown that H\textsubscript{2} not only acts as a co-catalyst to form surface-bound carbon species, but it also etches the weakly bonded carbon atoms from the graphene film. For this reason the final flakes are naturally grown in hexagonal shapes. Single crystallinity of the flakes is confirmed as identical SAED patterns are obtained at various examined locations on the surface of a particular hexagonal flake. D-band Raman map of two merged flakes show the existence of a GB in their merging region. 2D to G band ratio of the flakes also provides strong evidence that the flakes are indeed monolayer.
CHAPTER 3

THERMAL CONDUCTIVITY ACROSS AN INDIVIDUAL GRAPHENE GRAIN BOUNDARY AND SINGLE CRYSTALLINE CVD GROWN GRAPHENE

3.1 Introduction

Shrinkage in size of the carbon based nanoelectronics has led to nano-scale hot spots in device components. Formation of hot spots causes a concentration of all current at a particular spot and consequently breakdown of the system [48][49]. To explore these limitations, studies are done toward understanding the thermal transport in nanostructures. In particular, graphene has gained recognition not only for its outstanding electrical, but also for superior thermal properties. However, the electrical properties of graphene are shown to highly depend on the method to which the flakes are obtained. For instance extremely high electrical mobility of mechanically exfoliated graphene (~5000 cm²V⁻¹S⁻¹) is suppressed to a value <10³ for CVD graphene [37]. Likewise, it is expected to observe suppressed thermal conductivity in CVD grown graphene films.

Apart from the initial motivation for using graphene as a replacement for silicon in integrated circuits, graphene has also found great motivation in energy harvesting and recycling areas. In more details, giant thermoelectric potential have been predicted for graphene [50-52]. Thermoelectric materials are solid state devices that are capable of interconverting thermal energy to electrical potential and vice versa. The most efficient thermoelectric devices commercially available can only perform up to ~10% of the
Carnot cycle. The low efficiency in thermoelectric devices is due to the dimensionless Figure-of-Merit $ZT$ that governs the performance of these devices. $ZT$ is given as:

$$ZT = \frac{S^2 \sigma T}{\kappa_{\text{phonon}} + \kappa_{\text{electron}}} \quad (3.1)$$

Where $S$ is the Seebeck coefficient measured in $\Delta V/\Delta T$, $\sigma$ is the electrical conductivity, $T$ is the absolute temperature, and $\kappa_{\text{phonon}}$ and $\kappa_{\text{electron}}$ are the portions of thermal conductivity responsible by phonons and electrons, respectively. As it is clear from equation 3.1, the properties governing the efficiency of thermoelectric devices are partially dependent, yet in contradiction for achieving a high $ZT$. For instance, the ratio of $\sigma$ and $\kappa_{\text{electrical}}$ is limited by Wiedemann-Franz law given as:

$$\frac{\kappa_{\text{electrical}}}{\sigma} = LT \quad (3.2)$$

Where $L$ is a constant known as Lorenz number and is equal to $\sim 2.8 \times 10^{-8} \, W\Omega K^{-2}$. On the other hand, high $S$ requires a material with low carrier concentration and high effective mass, while a big $\sigma$ value necessitates exactly the opposite. The only parameter that is independent from the others is $\kappa_{\text{phonon}}$ which may be suppressed by engineering the nanostructures through implementation of imperfections such as grain boundaries. It is worth mentioning that thermal transport is graphene lattice is dominated by phonons rather than electrons [53]. Hence, suppression of $\kappa_{\text{phonon}}$ can effectively reduce the overall thermal conductivity of the structure resulting in a higher $ZT$. 

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The graphene films grown by CVD are mainly polycrystalline where single crystalline domains are joined by grain boundaries (GB). Existence of GB is theoretically predicted to create a sharp temperature drop across the graphene flake [54-56]. Since CVD graphene films contain many GB, the effect of GBs on the thermal transport is crucially important. However, no experimental work has yet quantified the thermal conductivity or the role of GBs on the thermal transport across the graphene lattice. Thus, motivated by the potential application of graphene in logic circuits and energy recycling areas, the thermal conductivity of single crystalline CVD graphene and the role of an individual GB on the overall thermal transport of the system are experimentally measured in this chapter.

3.2 Literature Survey

In this section, a brief survey over the methods previously used to extract thermal conductivity of carbon based nanostructures is provided. Thermal properties of a freely suspended single walled carbon nanotube (SWCNT) was first reported experimentally as ~3500 W/m.K by subjecting a SWCNT to relatively high electrical biases (>0.3 volts) which introduced joule self-heating into the SWCNT. Thermal conductivity was then extracted using the nonlinear trend seen in the current-voltage (I-V) curve of the system. This was done by solving for a thermal conductivity value that would regenerate the observed I-V trend [57]. There are several reports on the thermal properties of single and multilayered graphene obtained by the scotch tape method. One employed the
temperature dependence in G-peak position of the Raman signature of suspended single and few layered graphene. The reported thermal conductivity values are 4840-5300 W/mK and 3080-5150 W/mK, respectively [58][59]. Thermal transport of supported pristine graphene on SiO₂ substrate, however, was reported to be an order of magnitude smaller than the suspended value (~600 W/mK) [60]. This great suppression of thermal conductivity is explained by the interaction of the flexural mode of vibration in the graphene lattice (in the z-axis) and the phonon modes of the substrate resulting in scattering of the heat carriers. In another work, temperature dependence of graphene thermal conductivity ranging from 77K to 350K was studied by employing thermal bridge method. It was shown that thermal conductivity of the suspended samples follow a power law with an exponent of 1.4 ± 0.1. The deviation of the results from the theoretical values was attributed by phonon-boundary scattering at the supporting regions [61]. Similarly, by using heat spreader method Jang et al. [62] reported layer dependence of thermal conductivity of graphene encased by SiO₂ from both top and bottom interfaces. This study shed light into the single layer graphene to bulk graphitic thermal conductivity crossover. It was experimentally shown that the disruptions of thermal transport at the substrate/graphene interface affects the neighboring graphene layers up to around 2.5nm (7layers). In order to fully elucidate the physics behind changes in thermal transport regime going from single to few layered graphene, one carried out an experimental study on the dimensional crossover on multilayer graphene. It was reported that thermal conductivity decreases from ~2800 W/mK to ~1300 W/mK as the number of atomic
planes increases from 2 to 4. This phenomenon was explained by cross plane coupling of the low energy phonons and changes in the phonon Umklapp scattering resulted from crystal anharmonicity [63]. By employing high vacuum thermal microcopy imaging an effort was taken to study the local variation in thermal conductance of a suspended single and multi-layered graphene at different positions. Results revealed that thermal resistance is lower in the suspended area where the heat is conducted by ballistic phonons and in absent of electron scattering compared to areas adjacent to the supported region. They also indicated that the mean free path of thermal phonons in supported region is <100nm [64].

3.3 Nano-Scale Thermal Conductivity Measurement Platform

There are several technological difficulties toward measuring heat transfer in nano scale. In practice, in order to actually measure a temperature gradient across any structure, one needs to create the temperature gradient by dissipating a known amount of power in the system while simultaneously measuring the temperature between two points separated by a known distance. Having such measurement system on a material that is only one atom thick and is only few micrometers in length and width is very challenging. It should also be noted that fabricating a measurement platform for graphene on a typical SiO$_2$/Si substrate results in most of the heat being conducted through the substrate. This is mainly because the ratio of the cross-sectional area of graphene to that of a typical
substrate \( (A_{\text{substrate}}/A_{\text{graphene}}) \) is astronomical and performing a three dimensional heat transfer experiment for a two-dimensional material is not technologically feasible.

In this study, a measurement platform is designed to rule out most of the above difficulties in order to measure the thermal conductivity of single crystalline CVD graphene and a graphene lattice having just one GB. To this objective, a nano scale electrical heater and two thermometers are patterned using advanced electron beam lithography technique. The problems attributed to the supporting substrate are also ruled out by using a special substrate. The employed substrate contains a 75 \( \text{nm} \) Silicon Nitride (Si\(_3\)N\(_4\)) membrane grown on a 200 \( \mu \text{m} \) thick \(<100>\) oriented silicon substrate. A 500 \( \mu \text{m} \times 500 \mu \text{m} \) window is then thinned up to the 75 \( \text{nm} \) Si\(_3\)N\(_4\) layer leaving a wide enough and freely suspended substrate, confining the heat flow only to one dimension that is perfect for thermal conductivity measurement. The measurement platform and its corresponding thermal circuit are schematically shown in figure 3.1a and 3.1b. Similar platform have been previously employed by ref [65] for measuring the thermal conductivity of graphene nanoribbons, however, no free standing substrate was used in this study; therefore the reported measurements had up to 60% error. The electrical thermometry platform developed in this study is among the few measurement techniques that are applicable to nanostructures such as graphene. As demonstrated in figure 5a, the measurement platform consists of an electrical heater located at the center of the structure, and two electrical thermometers on the sides.
This platform can be divided into two regions. A single crystalline graphene flake covers the area between the heater and thermometer 1 (Th1), while two randomly merged flakes (forming a GB) cover the area between heater and thermometer 2 (Th2). In this configuration, it is possible to simultaneously measure the thermal conductivity of a single crystalline CVD graphene and the thermal conductivity of two graphene flakes having an individual GB. Figure 5b shows the equivalent thermal circuit of the designed platform. Device fabrication and experimentation details of the designed thermometry platform are discussed in the following sections.

Figure 5. (a) Schematic of the designed electrical thermometry platform on a suspended membrane. (b) Equivalent thermal resistance circuit of the platform.

### 3.4 Electrical Thermometry: Fabrication Process

Device fabrication for the designed thermometry platform on a freely suspended Si₃N₄ substrate requires special handling care since the 100nm Si₃N₄ is already
suspended and it is very easily broken. The fabrication process of our designed thermometry platform on such a thin substrate is described below.

Step 1. Substrate preparation: 200 μm thick 7.5 mm by 7.5 mm Silicon frames with a 500 μm × 500 μm suspended window of 75 nm Si₃N₄ are purchased from Silson Ltd. Substrates are cleaned in Piranha solution for 5 min, followed another by 5 min Deionized (DI) water bath. As described in chapter 2, precise control over growth condition in Ambient Pressure Chemical Vapor Deposition (APCVD) results in graphene flakes partially covering the surface of the copper foil in random positions. For this reason, prior to transferring graphene to the suspended Si₃N₄ substrate, the entire surface of the suspended window needs to be mapped with numbers (later referred to as alignment marks). The numbers are used both as alignment marks in the lithography processes and reference points to locate a suitable graphene flake over the surface. Alignment marks are patterned using Electron Beam Lithography system. Since the typical thickness of the e-beam resists is small, a bilayer PMMA e-beam resist system is employed in order to facilitate the lift-off process. A4 495K PMMA resist is initially spin coated on the substrate at 4000 rpm for 45 sec, and baked at 180°C on a hotplate for 90 sec. Next, A4 950K PMMA resist is spun on the substrate and baked in the same way. The sample is then loaded into Raith e-beam lithography system and the alignment mark patterns are written at 20 KV acceleration voltage and 120μm aperture size (typically resulting in ~5 nA beam current). The sample is then developed in a MIBK:Isopropanol(IPA) solution (1:3) for 1 min, rinsed with IPA immediately and
rapidly dried under N₂ flow. Afterward, a 5 nm of chromium (adhesion layer) followed by 40 nm gold is deposited on the substrate using Varian electron beam evaporation system. Lift-off process is performed in remover PG solution at ~70°C for 20-30 min followed by a 10 min of clean remover PG bath to ensure the removal of the entire metal particles from the surface. The samples are rinsed by Acetone and IPA and dried under N₂ flow.

**Step 2. Graphene transfer:** The graphene used in this study is grown using APCVD using the methods described in chapter 2. Partially covered hexagonal graphene flakes on copper are transferred to the prepared substrates by first spin coating the copper with a thick PMMA layer (A4 950K at 1500 rpm). The PMMA is left to dry under ambient conditions for ~3 hours and the copper foil is cut to proper size (fitting the substrate frame size). The graphene underneath the copper foil is then removed by floating them on a diluted Nitric Acid (1:3 in DI water) for 3 min. The foils are then transferred on a Ferric chloride CE-100 copper etchant solution in order to etch the copper away leaving only PMMA coated graphene floating on the solution. After ~8 hours the copper is completely etched away, using a clean piece of glass, the floating graphene/PMMA samples are taken out of the etchant solution and transferred to a DI water bath. At least two DI water baths are needed in order to clean the sample. Next, the samples are put in a Hydrochloric Acid (1:15 diluted in DI water) solution in order to remove the iron residues left from the copper etchant solution. After 15 min the samples are again cleaned in two DI water baths and are ready to be scooped out by a hydrophilic
receiving substrate. Transferring the samples to a hydrophobic substrate often creates a lot of folds and traps a lot of water molecules between the graphene and the substrate resulting in dirty unusable flakes. For this reason, the hydrophobic Si$_3$N$_4$ surface is dipped in a 1:100 diluted Buffered Oxide Etchant (BOE) solution for 15 sec and rinsed with DI water for 5 min. After this treatment, the Si$_3$N$_4$ substrates show decent hydrophilic properties. Hence the graphene/PMMA samples are scooped out of the DI water with the treated Si$_3$N$_4$ substrates. The samples are left to dry on air for ~1 hour, ramped up to 150°C on a hotplate over 10 min and left at 150°C to dry for another 10 min. This step is done not only to further dry the PMMA/graphene film on the substrate, but to ensure that the graphene is well adhered to the substrate before removing the PMMA. The PMMA is cleaned in acetone for 20 min, after which immediately transferred put in chloroform solution for 3 hours in order to clean the remaining PMMA residues. Finally, the graphene transferred to the substrate is rinsed with IPA and dried under N$_2$ flow. Before continuing for the rest of the fabrication process, the samples are annealed at 400°C under protection of Argon and Hydrogen for 3 hours. It should be noted that avoiding this step results in the graphene flakes either tearing apart or being completely remove from the substrate during the next lithography processes. Fundamental steps of the graphene transfer process are schematically demonstrated in figure 6.
Step 3. Grain boundary detection and definition: After the transfer and annealing processes, a pair of randomly merged graphene flakes need to be selected within the suspended Si$_3$N$_4$ window. Detection of graphene under optical microscope (OM) is possible by adjusting the colors, contrast, color temperature, saturation, and the illumination of the CCD camera. The value of the parameters greatly depends upon the thickness and the kind of the substrates since different substrates exhibit different color spectrums at a particular thickness. On the other hand, since we are only interested in the graphene flakes that are inside the suspended window area, this task becomes fairly more
complicated. Scanning Electron Microscope (SEM) is also an option for this step since graphene is much easier to spot under SEM. However, apart from the higher cost of this method, electron microscopy often results in creation of structural defects on the 2 dimensional materials (i.e. graphene, MoS$_2$). For this reason a $BX41TF$ Model optical microscope from Olympus with UM-Plan 10, 20, 50, and 100X objectives and a Pixelink $PL-B625CU-KIT$ CCD camera is employed for this step. By placing the Si$_3$N$_4$ samples on top of a Si/SiO$_2$ substrate and adjusting the CCD camera, the graphene flakes were successfully made visible in the suspended window area. Two randomly merged flakes are then located relative to the previously deposited alignment marks. At this point, the selected graphene flakes need to be protected while the rest of the flakes are etched away in an oxygen plasma cleaner system. An etch protection mask is patterned using the previously discussed EBL technique and bilayer PMMA resist system. After having the desired flakes protected with a bilayer PMMA resist, the rest of the flakes are burned away upon exposure to 100 W oxygen plasma and 350 $mTorr$ oxygen partial pressure for 3.5 min. The sample is then placed in a remover PG solution overnight for the etch mask to be removed. Figure 7 shows a pair of graphene flakes before and after the definition step.
Figure 7. Optical image of the selected graphene flakes before and after O\textsubscript{2} plasma etching step. Scale bars are 25 $\mu$m.

**Step 4. Electrode/Pad deposition and packaging:** Heater/thermometer electrodes are designed and patterned similar to the previously discussed EBL technique. Prior to the metal deposition, a 5 nm layer of SiO\textsubscript{2} needs to be deposited in order to prevent electrical contact between the electrodes and graphene. SiO\textsubscript{2} deposition is done using a CVC sputtering deposition system in RF mode. Prior to deposition the chamber is evacuated to $10^{-7}$ Torr using a cryopump. This is mainly done in order to remove any possible contaminants from the chamber. Argon gas is then purged into the system and the pressure is held constant at $\sim 10^{-3}$ Torr. After achieving the plasma, 5 nm SiO\textsubscript{2} is deposited at 200 W forward power for 90 sec. The samples are then loaded into Varian e-beam evaporation system where 5nm Titanium (adhesion layer) followed by 50 nm Platinum are deposited. Platinum is purposefully selected because of its higher temperature coefficient of resistance compared to gold. After the lift-off process, the samples are spin coated for the last time in order to pattern and deposit the pads. An
oxygen plasma cleaning step is done prior to metal deposition in order to make sure that there will be no graphene flakes trapped underneath the pads. Having graphene flakes under the pads usually weakens the adhesion between the metal and the substrate so that the pads cannot even survive the scotch tape test. It should also be noted that for packaging purposes (wire bonding) the pads must be made out of gold, which is why the electrode and the pad are not patterned in the same step. Final step toward the fabrication of the designed electrical thermometry platform is to package the fabricated chip by wire bonding it to a chip carrier. The chip is first glued to the chip carrier using a piece of copper tape. The wire bonding is then performed using a West Bond 7374E Wedge-Wedge wire bonder with low sonication power and bonding force on the pads. Figure 8a shows the SEM image of the graphene flakes used to fabricate the thermometry platform. The low quality of the image is due to electrical insulation of the Si₃N₄ substrate and very low acceleration voltage of the beam (5 KV). Figure 8b and 8c show the false colored SEM and optical image of the final device. The inset of figure 8b shows the final wire bonded chip. Once the chips are fabricated and packaged, electrical thermometry experiments are performed. Experimental setup and procedure are discussed in the following section.
Figure 8. (a) SEM image of the graphene flakes having a GB used for device fabrication. (b) False Colored SEM image of the final thermometry platform and picture of the final chip (inset). (c) Optical image of the final thermometry platform (d) Optical image of a typical broken device due to sudden discharge of electrostatic charges trapped in the wires.
3.4 Electrical Thermometry: Experimental Setup and Procedure

The resolution of electrical thermometry is directly influenced both by environmental conditions (vacuum level and temperature) and the level of electrical measurement capabilities of the setup. For this reason, in this study the experiments are done under high vacuum for temperatures ranging from 44K to 300K with nano volt sensitivity. In this section the experimental setup prepared and the electrical thermometry procedure are discussed in detail.

3.4.1 Experimental Setup

In order to measure the temperature dependence thermal conductivity of the fabricated graphene GB devices, a closed-cycle Cryostat model CCS-450 with a temperature range of ~10K to 500K and 52 feed-through pins is used from Janis Research Company. This system is equipped with an Edwards EXT75DX NW40 turbo-molecular pump station and a LakeShore model 335 temperature controller with an effective ±0.01K controlling resolution.

As the first step toward setting up this system, 24 twisted pair Polyimide insulated phosphor bronze 32 AWG wires are soldered to the feed-through pins inside the system. The other ends of the wires are soldered to a female socket chip carrier that couples with the male chip carriers prepared in the previous section. This design makes the task of establishing electrical contact with the loaded chip carrier very easy, without having to solder any wire to the delicate chip carriers. Figure 9a shows an image of the
female socket and the fabricated chip loaded into the Cryostat. An important criterion in designing the electrical connections inside a cryostat is that the wires can be a source of heat loss. To minimize this issue, a thermal anchor is embedded in the system by twisting the 24 wires around the top of the cold finger of the cryostat.

One common problem toward nano scale electrical measurement is that the electrostatic charge (EST) accumulated in the wires can easily blow the entire device as the chip is loaded into the system. Figure 8d shows a typical EST blown device. This issue becomes even more problematic in the case of nano-scale electrical thermometry of graphene since the mechanical strength and the adhesion of the electrodes are much weaker in the narrow electrodes.

In order to rule out this problem, a ground box is designed as illustrated in figures 9b and 9c. The two way switch in the box allows for grounding the wires to discharge the electrostatic charges while the π-filter between the switch and the cryostat filters any unwanted high frequency signals. In this way, before loading the sample all the wires will be grounded so that no sudden electrical current (spark) passes through the electrodes. However, even by using the ground box occasional device break-downs are observed that are probably from the operator or the charges trapped in the working area. The entire experimental setup is shown in figure 10.
Figure 9. (a) Picture of the chip-carrier mounted on the female chip carrier in the cryostat system. (b) Schematic of the ground box (c) Picture of the designed ground box.
The last step before carrying out the thermometry experiments is to calibrate the temperature of the Lakeshore 335 temperature controller with the actual temperature of the chip carrier mounted on the sample holder. In another word, a temperature drop between the temperature controllers’ sensor and the sample is expected since they are located around 3 cm apart. For this purpose, a surface mount CY7-SD cryogenic temperature silicon diode from Omega is employed to calibrate the system. In this experiment the temperature inside a chip carrier mounted on the sample holder is measured. The diode is mounted inside the chip carrier in the exact same way that a
fabricated chip would be. An Apiezon-N thermal grease from Janis is used on the back and inside the sides of the diode in order to improve the thermal contact resistance between sample holder and the chip carrier and also between the chip carrier and the sample. The system is then cooled down to 15K and ramped up to 305K by 10 degree increments. The temperature inside the chip carrier at each ambient temperature is measured by passing a constant 10 $\mu$A current through the diode and reading the corresponding potential drop. This measurement is done after waiting at least 10 minutes on each temperature for the cold finger to stabilize. The potential drop is then converted to temperature using the data sheet provided by the manufacturer. Significant temperature drop is observed in the chip carrier below ~190K. The temperature offset is increased at lower temperatures reaching a maximum of 29K at 15K. Figure 11 shows the calibration curve of the chip carrier’s temperature versus the cryostat temperature. This experiment is repeated 3 times and yielded identical curves at all runs.

Finally, the fabricated chip is carefully loaded into the calibrated cryostat after grounding all the wires. The chamber is then evacuated to $10^{-6}$ Torr and cooled down to 44K to start the electrical thermometry experiment. The temperature values in the following sections are the calibrated temperatures corresponding to the chip carrier.
3.4.2 Experimental Procedure

The principle of electrical thermometry is based on the change in the electrical resistance of the heater and the thermometer electrodes as their temperature is varied. Therefore, the change in electrical resistance of each electrode is first calibrated with temperature in a four probe configuration. A two channel Keithley 2612A source-meter is employed to monitor the resistance of the electrodes by apply a constant 1 µA current
as the temperature is ramped up from 44K to 305K. The constant 1 µA electrical current is carefully chosen in order to prevent joule self-heating during this process. By characterizing the temperature dependence of the electrodes, it is possible to monitor their temperature in the form of change in their electrical resistance. Figure 12a shows the calibration curves achieved in this step. The following quadratic relationships are found from the measurement:

\[ T_h(R) = 7.86 \times 10^{-5}R^3 - 25.97 \times 10^{-3}R^2 + 5.41103R - 273.55 \]  \hspace{1cm} (3.3)

\[ T_{\text{grain}}(R) = 2.47 \times 10^{-5}R^3 - 13.04 \times 10^{-3}R^2 + 3.97597R - 333.364 \]  \hspace{1cm} (3.4)

\[ T_{\text{GB}}(R) = 2.80 \times 10^{-5}R^3 - 19.56 \times 10^{-3}R^2 + 6.27755R - 652.268 \]  \hspace{1cm} (3.5)

Where \( T_h(R), \ T_{\text{grain}}(R), \ T_{\text{GB}}(R) \) are the temperatures of the heater electrode, grain electrode (thermometer 1) and GB electrode (thermometer 2) given as a function of their electrical resistance R. Figure 12b shows the room temperature I-V characteristic of the electrodes verifying perfect Ohmic-contact.
Figure 12. (a) Current-Voltage (I-V) characteristic of the electrodes. (b) Resistance of the electrodes as a function of ambient temperature inside the cryostat.
Next, the ambient temperature is held constant and a range of relatively higher electrical currents are passed through the heater electrode (by means of dissipating electrical power) while monitoring the resistance of the grain and GB thermometers. The electrical power \( P_h = RI^2 \) in the heater results in joule heating and changes its electrical resistance. The temperature rise in the heater (joule-heating) results in half of the heat being transferred to the grain electrode (through the single crystalline CVD graphene) and the other half to the GB electrode (through the graphene with GB). It is noted that due to the very small thickness of the substrate (75 nm), heat transfer is confined only to one dimension. Figure 13a shows the real time measurement of electrical resistance in the heater, grain and GB electrodes at 44K by applying different power values to the heater. The resistances are normalized by their initial values for consistency.

It is emphasized that a Keithley 6221/2182A combo is employed to monitor the electrical resistance of the right and left thermometer electrodes. A constant 1 µA current is passed through the electrodes as the resistance is measured in a four probe Delta Mode configuration in order to achieve ±5 nano volt precision. The change in the resistance of the electrodes shown in figure 13a is then converted to temperature rise using equations 3.3, 3.4 and 3.5. The temperature rise in the electrodes versus applied power to the heater at 44K background temperature is presented in figure 13b. However, the data corresponding to relatively lower electrical powers (10 to 25 µW) are used to extract the thermal conductivity values (later discussed in detail) as higher power values may result in too much temperature rise in the system that change the transport regime.
Figure 13. (a) Normalized change in the resistance of the electrodes as a function of heater power versus time at 44K ambient temperature. (b) Temperature rise in the electrodes as a function of applied power to the heater at 44K.

Knowing the temperature profile and the power dissipated into the system, the overall thermal conductance ($K_{overall}$) of the structure can be evaluated from the Fourier law of heat conduction:
$P = K_{overall} \frac{\Delta T}{\Delta x}$  \hspace{1cm} (3.6)

where $\Delta x$ is the length of the conduction channel. $K_{overall}$ represents both the heat conducted through the substrate and graphene structure, therefore it can be written as:

$$K_{overall} = \kappa_{\text{graphene}} A_{\text{graphene}} + \kappa_{\text{SiN}} A_{\text{SiN}} \hspace{1cm} (3.7)$$

where $\kappa_{\text{graphene}}$, $\kappa_{\text{SiN}}$, $A_{\text{graphene}}$ and $A_{\text{SiN}}$ are the thermal conductivity and cross-sectional area of graphene and Si$_3$N$_4$, respectively. In order to extract the thermal conductivity of our graphene structures, thermal conductivity of the substrate needs to be separately measured. For this reason, after this experiment the graphene is etched away through an O$_2$ plasma cleaning step and the sample is loaded back into the system. Similar experimental procedure is followed yielding $\kappa_{\text{SiN}}$ for all background temperatures. Finally, by subtracting the heat conduction through the substrate, the thermal conductivity of single crystalline CVD graphene and the role of an individual GB on the overall thermal conductivity of graphene are extracted from equation (3.7). 0.335 nm is assumed as the accepted value for the thickness of graphene [2].

### 3.5 Electrical Thermometry: Results and Discussions

Figure 15 shows the thermal conductivity of the single crystalline CVD graphene and graphene with individual GB as a function of ambient temperature from 44K to 305K. The room temperature thermal conductivity of single crystalline CVD graphene and graphene with a GB are measured as 1640 and 1300 W/m.K, respectively. The results
demonstrate that an individual GB reduces the thermal transport across the graphene lattice by approximately 26%. The downward temperature dependent trend in the thermal conductivity values is attributed to the reduction of available vibration modes as the temperature is cooled down. Also, the suppression of thermal conductivity in graphene having a GB is probably due to the defective nature of the GB that results in disruption of the lattice vibration (phonon transport) and scattering of the heat carriers.

The thermal resistance of GB region can be modelled as three thermal resistances in series as schematically shown below.

![Schematic of the thermal resistance model for two flakes having a GB.](image)

Knowing the thermal conductivity of the single crystalline graphene regions and the overall thermal resistance \(1/K_{\text{overall-GB}}\) of the region, it is possible to extract the thermal conductivity of the isolated GB for each ambient temperature using the following equivalent thermal resistance equations:

\[
R_{\text{overall-GB}} = R_{\text{graphene}} + R_{\text{GB}} + R_{\text{graphene}}
\] (3.8)
\[ R_{\text{overall-GB}} = \frac{L_{GR}}{\kappa_{\text{graphene}} A_G} + \frac{L_{GB}}{\kappa_{\text{GB}} A_{GB}} + \frac{L_{GL}}{\kappa_{\text{graphene}} A_G} \quad (3.9) \]

Where \( R_{\text{overall-GB}} \) is the overall thermal resistance of the GB region (graphene flakes having a GB), \( L_{GR}, L_{GL}, A_G \) are the lengths and cross-sectional area of the graphene regions on the right and left of the GB, respectively. Assuming a reasonable 3 nm average length for the GB (\( L_{GB} \)), and similar cross-sectional area (\( A_{GB} \)) to that of the graphene, the temperature dependent thermal conductivity (\( \kappa_{GB} \)) of an isolated GB are evaluated and shown in figure 16a. Also, the thermal conductance of the isolated GB (\( \frac{\kappa_{GB} A_{GB}}{L_{GB}} \)) is compared with the thermal conductance of a graphene film of similar geometry (3 nm long) as shown in figure 16b. The results are striking. The thermal conductivity and conductance of an isolated GB are around 3 orders of magnitude smaller than that of the graphene that is concentrated at a 3 nm region.

An equivalent thermal length of the GB defined as an extension in length of the graphene flake that would result in similar conductance is evaluated using the following relations:

\[
\begin{align*}
R_{GB} &= \frac{L_{\text{equivalent}}}{\kappa_{AG}} \\
R_{GB} &= \frac{L_{GB}}{\kappa_{GB} A_{GB}} \\
\Rightarrow \quad L_{\text{equivalent}} &= \frac{L_{GB} A_G \kappa_G}{\kappa_{GB} A_{GB}} \quad (3.10)
\end{align*}
\]

where \( L_{\text{equivalent}} \) is the equivalent thermal length of the GB. \( L_{\text{equivalent}} \) of the GB as a function of temperature is shown in figure 17a. Results indicate that the 3 nm long GB is
in fact equivalent to of 2.24 $\mu m$ of single crystalline CVD graphene that shrinks down to around 1.24 $\mu m$ at room temperature.

The measured temperature dependent thermal conductivity of 75 $nm$ Si$_3$N$_4$ is presented in figure 17b which is in good agreement with the previously reported values in the literature [66].

Figure 15. Measured temperature dependent thermal conductivity of single crystalline CVD graphene and graphene flakes with an individual GB
Figure 16. (a) Temperature dependent thermal conductivity of an isolated GB. (b) Temperature dependent thermal conductance of a 3 nm isolated GB and 3 nm single crystalline graphene.
Figure 17. (a) Equivalent thermal length of an isolated GB (b) Temperature dependent thermal conductivity of the 75 nm Si$_3$N$_4$. 
3.6 Conclusion

An electrical thermometry platform is designed on a suspended silicon nitride membrane. Electron beam lithography together with standard electron beam evaporation, RF sputtering deposition, and plasma cleaning techniques are employed to fabricate the platform on a single crystalline CVD grown graphene flake and a graphene flake having an individual grain boundary. The temperature dependence in thermal conductivity of single crystalline graphene and graphene with grain boundary is measured from 44K to 305K. It is shown that existence of grain boundary results in around 26% reduction in the overall thermal conductivity of the graphene lattice. In more details, the thermal conductivity of an isolated GB is extracted to be around 3 orders of magnitude smaller than the single crystalline graphene lattice. Also, the equivalent thermal length of the GB is evaluated for the entire ambient temperature range. It is shown that an individual GB that is around 3 nm in length, in fact acts like a 2.24 μm of single crystalline graphene at 44K that shrinks down to 1.24 μm at room temperature.

The findings in this work are critically important for understanding the thermal transport across polycrystalline CVD graphene films. Also, another major impact of this study lies within the fact that by controlling the position and the density of GBs in a graphene film, it is possible to tailor the thermal properties of graphene which is a step further toward phonon engineering and design of efficient thermoelectric materials.
CHAPTER 4

CONCLUSION AND FUTURE STUDIES

In this study, large area single crystalline hexagonally-shaped graphene flakes are grown on copper foil using Atmospheric Pressure Chemical Vapor Deposition system. Graphene grown using this method is ideal for fundamental research studies on graphene grain boundaries since the GBs are simply formed at the merging region of two hexagons. Merging region of two hexagonal flakes can be easily spotted using a simple optical microscope in the Dark-Field mode. Therefore, one of the greatest technological difficulties toward the study of GBs, which is finding the GBs using a non-destructive method, is resolved. Raman spectroscopy shows that the graphene grown using this method are high quality single crystalline flakes having a defective structure at their merging region. The defective nature of the merging region confirms that there exists a GB at the merging region of two merged flakes.

Thermal conductivity of a single crystalline graphene flake and the role of an individual graphene GB on the thermal transport across the graphene lattice are experimentally measured. An electrical thermometry is designed to simultaneously measure the thermal conductivity of the single grain and the grain boundary regions of two randomly merged graphene flakes. The platform is fabricated on a 75 nm thick free standing Silicon Nitride (Si$_3$N$_4$) membrane using electron beam lithography and other micro-fabrication techniques. The free standing Si$_3$N$_4$ is purposefully selected in order to
confine the heat flow only to one dimension, hence simplifying the measurement. The
temperature dependence thermal conductivity of the sample are measured from 44K to
room temperature. It was shown that an individual grain boundary is equivalent to around
1.24 \( \mu m \) of single crystalline graphene and reduces the thermal conductivity of the
samples by \(~26\%\). The room temperature thermal conductivity of single crystalline CVD
graphene and graphene with a GB are measured as 1640 and 1300 W/m.K, respectively.

A great improvement to this study is to perform quantum modeling and analysis
in order to understand the mechanism responsible for phonon scattering at the GB. The
designed thermometry platform and fabrication techniques are also applicable to other
two dimensional materials such as Molybdenum Disulfide (MoS\(_2\)) or Tungsten(IV)
sulfide (WS\(_2\)).
CITED LITERATURE


CITED LITERATURE (continued)


CITED LITERATURE (continued)


CITED LITERATURE (continued)


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